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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,781	04/09/2004	Shunpei Yamazaki	0756-7289	8829

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ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,781	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-42 and 45-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33-42 and 45-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 6/12/06. Currently, claims 33-42 and 45-63 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 33, 34, 37-42, 45-47, 49-52, 54, 55, 57-59 and 61-63 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al., US Patent 6,737,306

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Yamazaki discloses the semiconductor method as claimed. See figures 1A-16B and corresponding text, where Yamazaki teaches, pertaining to claim 33, a method for manufacturing a thin film transistor comprising the steps of: forming a crystalline semiconductor film **102-105** by irradiating an energy beam output continuously while scanning the energy beam to a

semiconductor film (figures 1A and 14; col. 7, lines 28-33 and 39-45); forming a gate electrode **122-125** over a portion of the crystalline semiconductor film which is included in an element-forming region (figures 1B and 1D; col. 8, lines 50-52 and 17-21); and forming an impurity region **118-121** in the crystalline semiconductor film using the gate electrode as a mask (figure 1C; col. 9, lines 39-56), wherein a scanning direction of the beam changes outside the element-forming region (figure 14; col. 7, lines 59-65).

Yamazaki teaches, pertaining to claim 34, a method for manufacturing a thin film transistor comprising the steps of: forming a crystalline semiconductor film **102-105** by irradiating an energy beam output continuously while scanning the energy beam to a semiconductor film (figures 1A and 14; col. 7, lines 28-33 and 39-45); forming a gate electrode **122-125** over a portion of the crystalline semiconductor film which is included in an element-forming region (figures 1B and 1D; col. 8, lines 50-52 and 17-21); and forming an impurity region **118-121** in the crystalline semiconductor film using the gate electrode as a mask (figure 1C; col. 9, lines 39-56), wherein the beam starts irradiation from outside the element-forming region or ends irradiation outside the element-forming region (figure 14; col. 7, lines 59-65).

Yamazaki teaches, pertaining to claims 37 and 38, wherein the energy beam output continuously is a beam emitted from a laser selected from the group consisting of a YVO_4 laser, a YAG laser, a YLF laser, a $YALO_3$ laser, and an Ar laser (col. 7, lines 39-45).

Yamazaki teaches, pertaining to claims 39 and 40, wherein the element-forming region is a region where a display device or an integrated circuit is formed (col. 13, lines 8-14).

Yamazaki teaches, pertaining to claim 41, a method for manufacturing a semiconductor device comprising the steps of: forming a semiconductor film **102-105** over a substrate **100**

(figures 1A; col. 7, lines 28-33); crystallizing the semiconductor film **102-105** by irradiating an energy beam output continuously while scanning the energy beam to the semiconductor film (figures 1A and 14; col. 7, lines 28-33 and 39-45); forming a plurality of semiconductor islands by patterning the crystallized semiconductor film (figure 1A; col. 7, lines 28-33); forming a first circuit **202** using one of the plurality of semiconductor islands over the substrate (figure 3B ; col. 13, lines 8-14); and forming a second circuit **205** using another one of the plurality of semiconductor islands over the substrate (figure 3B ; col. 13, lines 8-14), wherein the energy beam is not irradiated to the first circuit and the second circuit whiling changing a scanning direction of the energy beam (figure 14; col. 7, lines 59-65).

Yamazaki teaches, pertaining to claim 42, wherein the energy beam is irradiated to a region between the first circuit and the second circuit while changing the scanning direction of the energy beam (figure 14; col. 7, lines 59-65).

Yamazaki teaches, pertaining to claims 45-47, wherein the semiconductor device is incorporated into at least one selected from the group consisting of a display, a mobile computer, a game machine, and an electronic book reader (col. 18, lines 29-40).

Yamazaki teaches, pertaining to claim 49, wherein the energy beam output continuously is a beam emitted from a laser selected from the group consisting of a YVO_4 laser, a YAG laser, a YLF laser, a $YALO_3$ laser, and an Ar laser (col. 7, lines 39-45).

Yamazaki teaches, pertaining to claim 50, a method for manufacturing a semiconductor device comprising the steps of: forming a semiconductor film **102-105** over a substrate **100** (figure 1A; col. 7, lines 28-33); crystallizing the semiconductor film **102-105** by irradiating an energy beam output continuously while scanning the energy beam to the semiconductor film

(figures 1A and 14; col. 7, lines 28-33 and 39-45); forming a plurality of semiconductor islands by patterning the crystallized semiconductor film (figure 1A; col. 7, lines 28-33); forming a first circuit **202** using one of the plurality of semiconductor islands over the substrate (figure 3B ; col. 13, lines 8-14); and forming a second circuit **205** using another one of the plurality of semiconductor islands over the substrate (figure 3B; col. 13, lines 8-14), wherein the energy beam starts irradiation from outside of the first circuit and the second circuit or ends irradiation outside the first circuit and the second circuit (figure 14; col. 7, lines 59-65).

Yamazaki teaches, pertaining to claim 51, a method for manufacturing a thin film transistor comprising the steps of: forming a crystalline semiconductor film **102-105** by irradiating an energy beam output continuously while scanning the energy beam to a semiconductor film by moving the semiconductor film and the energy beam relatively (figures 1A and 14; col. 7, lines 28-33 and 39-45); forming a gate electrode **122-125** over a portion of the crystalline semiconductor film which is included in an element-forming region (figures 1B and 1D; col. 8, lines 50-52 and 17-21); and forming an impurity region **118-121** in the crystalline semiconductor film using the gate electrode as a mask (figure 1C; col. 9, lines 39-56), wherein a scanning direction of the beam changes outside the element-forming region (figure 14; col. 7, lines 59-65).

Yamazaki teaches, pertaining to claim 52, a method for manufacturing a thin film transistor comprising the steps of: forming a crystalline semiconductor film **102-105** by irradiating an energy beam output continuously while scanning the energy beam to a semiconductor film by moving the semiconductor film and the energy beam relatively (figures 1A and 14; col. 7, lines 28-33 and 39-45); forming a gate electrode **122-125** over a portion of the

crystalline semiconductor film which is included in an element-forming region (figures 1B and 1D; col. 8, lines 50-52 and 17-21); and forming an impurity region **118-121** in the crystalline semiconductor film by using the gate electrode as a mask (figure 1C; col. 9, lines 39-56), wherein the beam starts irradiation from outside the element-forming region or ends irradiation outside the element-forming region (figure 14; col. 7, lines 59-65).

Yamazaki teaches, pertaining to claims 54, 57 and 61, wherein the energy beam output continuously is a beam emitted from a laser selected from the group consisting of a YVO_4 laser, a YAG laser, a YLF laser, a $YALO_3$ laser, and an Ar laser (col. 7, lines 39-45).

Yamazaki teaches, pertaining to claims 58 and 62, wherein the element-forming region is a region where a display device or an integrated circuit is formed (col. 13, lines 8-14).

Yamazaki teaches, pertaining to claims 55, 59 and 63, wherein the semiconductor device is incorporated into at least one selected from the group consisting of a display, a mobile computer, a game machine, and an electronic book reader (col. 18, lines 29-40).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 35, 36, 48, 53, 56 and 60, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., US Patent 6,737,306 in view of Wu US Patent 4,439,245.

Yamazaki discloses the semiconductor method substantially as claimed. See preceding rejection of claims 33, 34, 37-42, 45-47, 49-52, 54, 55, 57-59 and 61-63 under 35 U.S.C. 102(e).

However, Yamazaki fails to show, pertaining to claims 35, 36, 48, 53, 56 and 60, wherein scanning the energy beam is performed by using a galvanometer mirror or a polygon mirror.

Wu teaches, a similar method of crystallizing a semiconductor film using a continuous wave laser, such as a Nd:YAG laser, that includes the use of a galvanometer for driving the beam to a desired scanning direction (col. 3, lines 25-47; col. 6, lines 13-16).

It would have been obvious to one of ordinary skill in the art to incorporate, wherein scanning the energy beam is performed by using a galvanometer mirror or a polygon mirror, in the method of Yamazaki, pertaining to claims 35, 36, 48, 53, 56 and 60, according to the teachings of Wu, with the motivation that, by including a galvanometer mirror within an optical system of a laser beam apparatus, the scanning direction of the laser beam is more accurately controlled, resulting in a uniformed annealing process of the semiconductor film.

Response to Arguments

Applicant's arguments, see Remarks, filed 6/12/06, with respect to the rejection(s) of claim(s) 33-42 and 45-63 under 35 U.S.C. 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Yamazaki et al., US Patent 6,737,306 under 35 U.S.C 102(e) and Yamazaki et al, US Patent 6,737,306 in view of 4,439,245.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
August 10, 2006

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812